Amendments To The Specification:

In the English translation document, please delete the term --Description-- at page 1 line 1, before the title.

In the English translation document, please add the paragraph at page 1 line 5, after the title, as follows:

--CROSS REFERENCE TO RELATED APPLICATIONS

This application is the US National Stage of International Application No. PCT/EP2003/008794, filed August 7, 2003 and claims the benefit thereof. The International Application claims the benefits of European application No. 02020602.5 filed September 12, 2002 and European application No. 02027848.7 filed December 12, 2002, all of the applications are incorporated by reference herein in their entirety.--

In the English translation document, please add the paragraph at page 1 line 5, after the newly added CROSS REFERENCE TO RELATED APPLICATIONS section, as follows:

--FIELD OF INVENTION

This invention relates to a method, processor and computer system for synchronizing external events for redundant processors.--

In the English translation document, please add the section heading at page 1 line 5, after the newly added FIELD OF INVENTION section, as follows:

--BACKGROUND OF INVENTION--

In the English translation document, please add the section heading at page 4 line 25, as follows:

--SUMMARY OF INVENTION--

In the English translation document, please amend the paragraph at page 5 lines 1-5, as follows:

This object is achieved by a method for synchronizing external events according to the features of ~~Claim 1~~the Claims, by a processor according to the features of ~~Claim 6~~the Claims

and by a system according to the features of ~~Claim 7~~ the Claims. Advantageous developments are specified in the dependent Claims.

In the English translation document, please add the section heading at page 8 line 5, as follows:
--BRIEF DESCRIPTION OF THE DRAWINGS--

In the English translation document, please add the section heading at page 8 line 14, as follows:
--DETAILED DESCRIPTION OF INVENTION--

In the English translation document, please amend the paragraph at page 10 lines 8-29, as follows:
The inventive method can be implemented directly as an instruction sequence, i.e. as software, based on the operation shown. The software thereby ensures that an interrupt is presented at identical points in the command execution of a plurality of processors, by programming an instruction counter in the CPU so that it prompts an exception, e.g. a debug exception, or a high-priority, non-blockable interrupt, e.g. the non-maskable interrupt NMI, after the required number MIC of instructions to be processed minus the "interrupt indeterminacy" MD. For example with an indeterminacy of MD = 3 instructions and a required number of MIC = 1000 instructions, the counter IC is programmed with 1000-3+1=998. Depending on the internal grouping of instructions, the CPU is therefore stopped after IC=998 or IC=999 or IC=1000 instructions. The software then ~~run~~ reads the instruction counter to determine at which point the processor actually stopped. This software is thereby set up so that the execution of its own instructions is corrected accordingly. If the software determines that the CPU has stopped for example after 999 instructions, the required 1000th instruction is executed subsequently by single step operation, controlled by the exception software. This happens with all redundant CPUs, so that all CPUs have then been stopped at the identical point in the code.